WORKSHOP
ON
EMERGING TRENDS IN VLSI
[ETV 2014]

Registration Form:

Name (In capital letters): .....
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Designation: .....
.....
Organization: .....
.....
Address for correspondence: .....
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.....
Mobile No. : .....
Email id :.....
Registration Fees: .....
D.D. No:.....
Date:.....

Click whichever applicable :

- ❑ Faculty
- ❑ Participants form R&D Inst.
- ❑ Research Scholar
- ❑ Post Graduate Student
- ❑ Industry & Other

Place: .....
Date: ..... Signature of Applicant

SPONSORSHIP CERTIFICATE

The applicant is hereby sponsored and will be permitted to attend the above short term course, if selected.

Date: **Signature and seal of the sponsoring authority**

Who can attend ETV2014

ETV 2014 is aimed to attract and bring together Faculty Members, Teaching Assistants and Research Scholars from Academic and Institutions recognized by AICTE, UGC or equivalent.

How to apply

Registration fee by Demand Draft in favour of Director NIT Durgapur payable at Durgapur along with duly filled in registration form should reach the convenor(s) on or before 31st January, 2014. Photocopy of the registration form can be used for registration. A confirmation mail will be sent to each registered participant by 31st January 2014.

Registration Fee

Faculty from Academic Institution:	INR 2000
Participants from R&D Institution :	INR 4000
Research Scholars :	INR 2000
Post-graduate students:	INR 2000
Participants from Industry and other organizations :	INR 6000

Patron:

Prof. T. Kumar, Director NIT Durgapur

Advisory Committee:

Prof. P. P. Gupta, Dean, (R & D)
Prof. K. C. Ghanta, Coordinator, TEQIP-II
Prof. B. Halder, Nodal Officer, TEQIP-II
Prof. G. Sanyal, Dean (Student Welfare)

Important Dates:

Last date of application submission:	31st Jan, 2014
Date of Notification (web):	5th Feb, 2014
Date of confirmation (email):	7th Feb, 2014

Contact person:

Dr. Suchismita Roy, 9434788122, suchismita27@yahoo.com
Mr. Bibhash Sen, 9434788161, bibhash.sen@cse.nitdgp.ac.in

Address for correspondence

Department of Computer Science and Engineering
NIT Durgapur
Mahatma Gandhi Avenue,
Durgapur-713209
Email: **etv2014.nitdgp@gmail.com**

TEQIP-II SPONSORED

WORKSHOP
ON
EMERGING TRENDS IN VLSI
[ETV 2014]

17-21 FEBRUARY, 2014

Course Coordinators:
Dr. Suchismita Roy
and
Mr. Bibhash Sen

Organized By

Department Of Computer Science and Engineering

NATIONAL INSTITUTE OF TECHNOLOGY DURGAPUR

Mahatma Gandhi Avenue Durgapur – 713209
West Bengal, India
Website: www.nitdgp.ac.in

About the institute

National Institute of Technology (NIT) Durgapur is a leading institute offering undergraduate, post graduate and post-doctoral programs in various disciplines of engineering, technology, science, social science and management. The education system is holistic with equal importance being attached to all-round development of the students. NIT Durgapur was established as a Regional Engineering College (REC) in 1960 as a joint venture of the Government of India and Government of West Bengal. REC Durgapur was converted to NIT Durgapur under the full administrative and financial control of the Ministry of Human Resource Development of the Government of India with a Deemed University status on 3rd July, 2003. Subsequently NIT Durgapur has been given the status of a University by the UGC Act. The Institute was declared as an Institute of National importance by The Government of India on 15th August, 2007.

About the workshop

The computer and electronics revolution we are witnessing today is driven by market demands to provide better, cheaper, smaller and faster products while meeting users' quality requirements. Meeting these quality requirements necessitates adequate reliable design procedures. This workshop concentrates on the dynamic changes in the VLSI design industry and its development, manufacture, test, diagnosis and verification of complex new chips with an objective to provide a forum to exchange ideas, discuss solutions, and study the electronics industry and its impact on products. Being able to rapidly develop, manufacture, test, diagnose and verify complex new chips and products using such chips is crucial for the continued success of our economy at-large. This growth is expected to continue full force at least for the next decade, while making possible the production of chips at nanoscale. The semiconductor industry is at a turning point. Keeping this in mind we propose to conduct a workshop on Emerging Trends in our experiences with researchers, professionals, and application developers working or planning to initiate research in this domain of computer architecture and VLSI design.

Topics to be covered

1. **Biochip**: Emerging technology of droplet-based micro fluidic labs-on-a-chip and walk through their recent developments and applications to various medical and healthcare systems, such as clinical diagnosis, point-of-care medical assistance, and DNA analysis. In order to fabricate such a biochip, one has to design a micro fluidic platform and integrate it with a microcontroller and on-chip electronic/optical sensors. We will focus on several resource optimization and reliability issues that need to be addressed while designing them. In particular, we will demonstrate, with a few examples, how these devices can be efficiently used for implementing real-life biochemical protocols on-chip and for drug delivery.
2. **Cellular Automata**: As the semiconductor technology is moving towards the submicron era, the system designers try to embed complex functions from software domain to hardware blocks on the silicon floor. At the same time for keeping the design complexity within a feasible limit, the designers are forced to look for simple, regular, modular, cascadable, and reusable building blocks for implementing various complex functions. The homogeneous structure of cellular automata (CA) is a right candidate to fulfill all the above objectives
3. **Quantum-dot cellular automata**: One of the most promising nanotechnologies which can replace the present transistor based CMOS technology is the Quantum-Dot Cellular Automata. The major advantages of this technology are lesser power dissipation, improved speed and dense structures. Logic Design with Quantum Dots is one of the most recent technologies being researched which allows scaling to continue to atomistic dimensions. Owing to electron repulsion and Coulomb blockade electrons are aligned automatically such that the energy of the system is minimum.
4. **VLSI design**
5. **Formal verification**

Resource person

1.	Dr. P P Chakrabarti	IIT Kharagpur
2.	Dr. B Bhattacharjya	ISI Kolkata
3.	Dr. B K Sikdar	BESU Shibpur
4.	Dr. A Mondal	IIT Patna
5.	Dr. G Sanyal	NIT Durgapur
6.	Dr. S Roy	
7.	Dr. D Mitra	
8.	Ms M Saha	
9.	Ms M Dalui	
10.	Mr B Sen	

Accommodation:

Boarding, lodging and travel expenses shall be borne by the participants. Limited shared accommodations can be made (on request) in the Institute Guest House (if available) on first come first served basis. Several good hotels are available in and around Durgapur. Participants may contact directly or through the coordinator(s) for accommodation in Guest House/Hotels. No TA/DA will be paid to the participants by NIT Durgapur.