National Institute of Technology
Durgapur, India

NXP
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End-to-End Mixed Signal Chip Design

August 5, 2015
National Institute of Technology Durgapur, India

The Department of Electronics & Communication Engineering (ECE) at National Institute of Technology Durgapur, in collaboration with NXP Semiconductors Bangalore, is pleased to announce a Workshop on End-to-End Mixed Signal Chip design, to be held on August 5, 2015 in NIT Durgapur. Mr. Abhijit Dutta and Mr. Hitesh Garg are among the notable speakers in the workshop.

An IC chip is broadly defined as a very-large-scale-integration of electronic components to realize a function as part of the system. In a Mixed Signal IC design, typically Digital and analog functions are put together on the same Silicon substrate. This category of chip has grown dramatically with the increased use of 3G cell phones and other portable technologies. Mixed-signal ICs are often used to convert Analog signals to Digital signals so that Digital devices can process them. For example, mixed-signal ICs are essential components for FM tuners in Digital products such as media players, which have Digital amplifiers. Any Analog signal can be Digitized using a very basic Analog-to-Digital converter, and the smallest and most energy efficient of these would be in the form of mixed-signal ICs. Mixed-signal ICs are more difficult to design and manufacture than Analog-only or Digital-only integrated circuits. For example, an efficient mixed-signal IC would have its Digital and Analog components share a common power supply. However, as one can imagine, Analog and Digital components have very different power needs and consumption characteristics that make this a non-trivial goal in chip design.

The focus of this workshop is to introduce students and researchers to the challenges of latest CMOS IC design flow both in Analog and Mixed Signal domain. There are competing IC technologies that aim to improve the performance aspects like power, noise and reliability. An understanding of different options, their pros and cons, as well as the associated tradeoff issues are important and is the goal of this workshop.

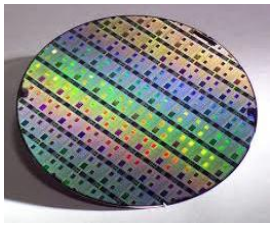
This workshop will be organized around the following sessions:

- Complete Chip Design Flow
- Analog Design Techniques
- ARM Embedded development Systems
- Opportunities for NXP-NITD Collaboration

Each session will consist will of 1.5-2 Hrs duration. The last session will identify specific opportunities and recommendations for NIT Durgapur VLSI Chip design activities.

Please mark your calendar for this event and contact Prof. Ashis K. Mal, Prof. Rajat Mahapatra (a.k.mal@IEEE.org : 94-347-880126), if you are interested in participation. To register online, please use the form http://goo.gl/forms/BjnzohAhJv For more information visit: http://ece.nitdgp.ac.in

Support for the workshop is provided by TEQIP-II of the Institute.



TEQIP-Phase II,
NIT Durgapur

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Distinguished Speakers

Abhijit Dutta has long experience in Semiconductor Industry with focus on ASIC / SoC Physical Design. Built large teams from scratch and brought them to a level of highly performing teams. Broad experience in R&D / Product development setups, including system level designs. More than 12 years of working with global teams spread across mainly in the USA & Europe. Built over time, personalized management style which bonds people together resulting in team achievements in the next level.

He is now Department Manager of the NXP Bangalore group working on end-to-end product in High Voltage Analog Mixed Signal chips. The group is part of Automotive Business Unit. Current focus is Solid State Lighting for Automotive applications, In-Vehicle Networking (CAN/LIN products) and Sensors (Speed, angle)

Specialties: Physical Design, DFT, Interface (I/O) design, System Level & Board Level Design

Hitesh Garg holds the role of Department Manager, AMSIP in NXP Semiconductors, India. In this role, he is responsible for building world class AMS IPs for NXP Products. In addition, he is also managing the Analog and Mix Signal competency at NXP India. His teams is busy in designing differentiating IPs/Products in areas of Data Convertor, Accurate References and Power Management. Hitesh also drives Data Convertor IP Portfolio Developments for all the NXP Business needs. Hitesh has more than 19 years of experience in Analog Mixed signal IP/product development. He joined NXP in 2008 while NXP acquired STB business from Conexant. At Conexant, his team contributed to the success of multiple Analog IPs and SoC products in Set Top Box and Broadband Access areas. Prior to Conexant, Hitesh has worked in Microchip Technologies and State owned Semiconductor Complex Limited in various technical and lead roles. Hitesh holds a Bachelors degree in Electronics & Communication and a Post Graduate Degree in Management from IIM Bangalore.

Functional area: Engineering Design / R and D and Heading Analog Mixed Signal Group.