EECS240 – Spring 2010

Advanced Analog Integrated Circuits
Lecture 1: Introduction

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Course Focus

- **Focus is on analog design**
  - **Typically: Specs → circuit topology → layout**
- **Will learn spec-driven approach**
  - **But will also look at where specs come from**
- **Key point:**
  - **Especially in analog, some things are much "easier" to do than others**
  - **Sometimes the right thing to do is change the specs**

Course Goal

- **Learn how to create systematic approaches to analog design**
  - **Based on fundamental principles**
  - **For a wide variety of applications**

- **Will show specific design methodology example**
  - **OTA designs embedded in ADCs**

Administrative

- **Course web page:**
  Use bspace for all class communications (bspace.berkeley.edu)

- **Webcast link:**
  http://webcast.berkeley.edu

- **Office hours**
  - **Tues. and Thurs. 11am-12pm (right after class)**
- **All announcements made through bspace**

Lecture Notes

- **Based on material from (myself,) Prof.E.Alon, Prof. Bernhard Boser, and Prof. Ali Niknejad**
- **Primary source of material for the class**
  - **No required text – reference texts on next slide**
- **Notes posted on the web at ~ 1 hour before lecture**

Reference Texts

- **Analysis and Design of Integrated Circuits,**
  Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, 4th Ed., Wiley, 2001.

- **Design of Analog CMOS Integrated Circuits,**
  Behzad Razavi, McGraw-Hill, 2000.

- **The Design of CMOS Radio-Frequency Integrated Circuits,**
  Thomas H. Lee, 2nd Ed., Cambridge University Press, 2003.
- **Analog Integrated Circuit Design,**
  K.Martin, C. Carusone and D. Johns, 2e, Wiley, 2013.
- **The Designers Guide to SPICE & SPECTRE,**
  K. S. Kundert, Kluwer Academic Press, 1995**.**
- **Operation and Modeling of the MOS Transistor,**
  Y. Tsividis, McGraw-Hill, 2nd Edition, 1999**.**
- **Nanometer CMOS ICs : From basics to ASICs,**
  Harry J.M. Veendrik, Springer, 2nd Edition, 2017**.**

Grading

- **Grading:**
  - **HW: 20%**
    - **One HW roughly every two weeks**
    - **Essential for learning the class material**
    - **Need to setup HSPICE or equivalent simulator (SpectreRF, Eldo, or other favorite tool)**
  - **Project: 25%**
    - **Groups of 2 – find a partner ahead of time**
  - **Midterm: 20%**
  - **Final Exam: 35%**

Homework

- **Homework:**
  - **Can discuss/work together**
  - **But write-up must be individual**
  - **Drop in EE240 drop-box**
  - **Generally due 5pm on Thursdays**

- **<u>No</u> late submissions**
  - **Start early!**

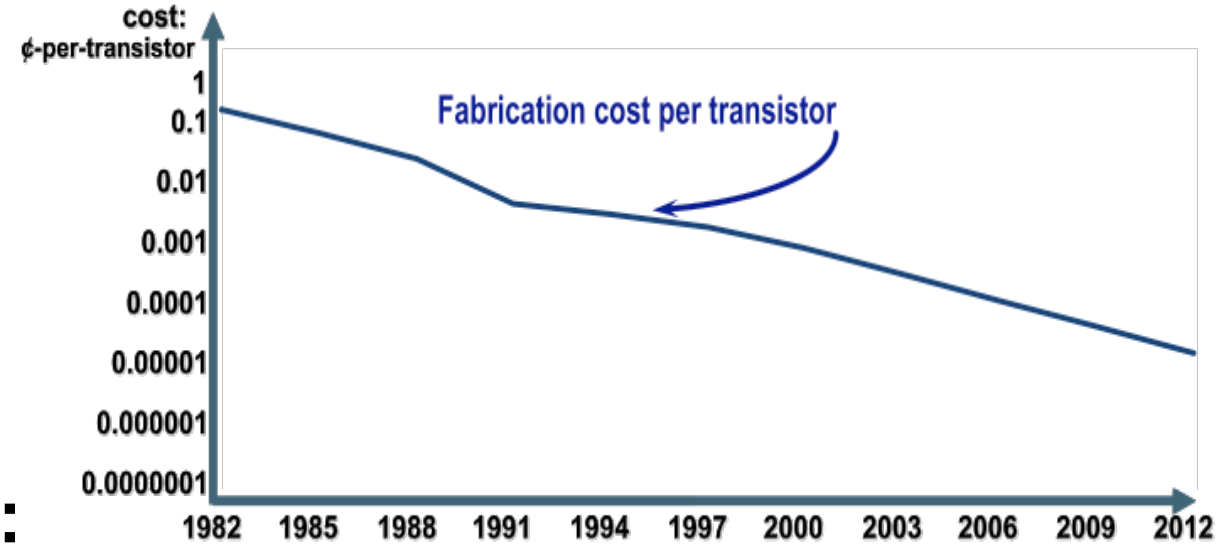
Schedule Notes

- **ISSCC Week: 2/20 – 2/24 (no lectures)**
- **Midterm: March 11 (tentative)**
- **Spring break: 3/21 – 3/25**
- **Project:**
  - **Start After Midterm, Due May 6 (tentative)**
- **Final: Wed., May 11, 11:30am-2:30pm**

"Analog ICs in a Digital World?"

Digital circuitry:

- Cost/function decreases by 29% each year
- 30X in 10 years



Analog circuitry:

- Cost/function may not scale very well
- Common complaints about scaling analog:
  - Supply voltage is too low, device gain is low, horrible matching…

"Analog will die – everything will be digital!"

- Who agrees?

(Good) Digital Design Needs Analog Insights

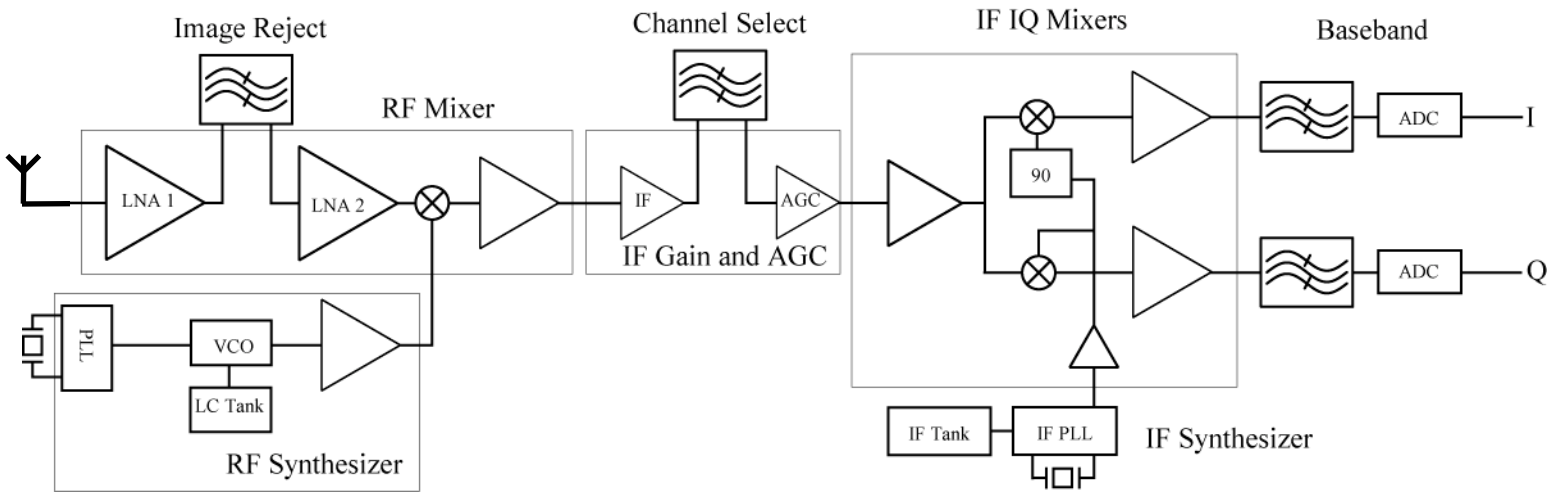
- Can synthesize large blocks at “medium” frequencies in ASIC flow, but
  - Need to know transistors to design the cells
  - Really need to know transistors to design memories
- Lots of analog issues to deal with when push digital performance, power, etc.
  - Charge sharing, interconnect parasitics, etc.
- Matching growing concern in advanced CMOS technologies
  - Especially in memories

The More Fundamental Reason

- The “real” or “physical” world is analog
  - Analog is required to interface to just about anything
    - Digital signals have analog characteristics too…
  - In many applications, analog is in the critical path

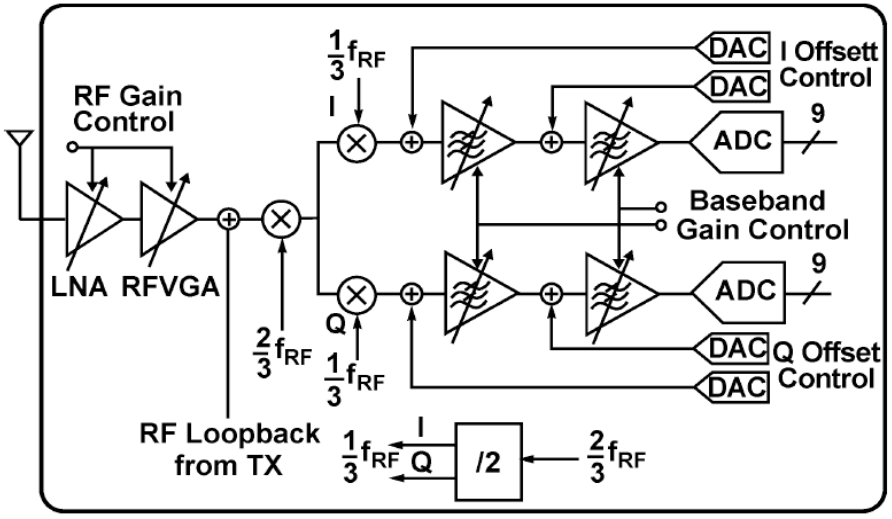
- Examples:
  - Wireline, optical communications
  - RF transceivers (receiver + transmitter)
  - Sensors and actuators (e.g., MEMS)

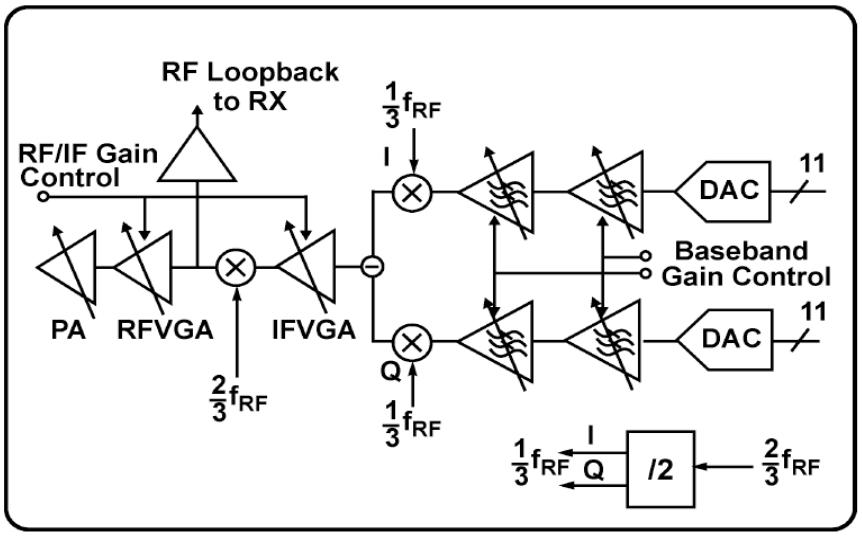
RF Receiver

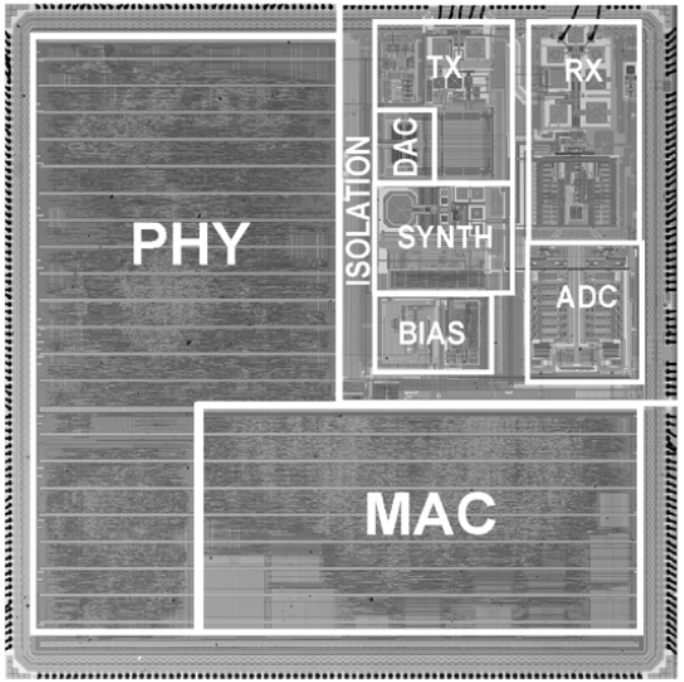


- **Why so many RF and analog building blocks?**
- **Why not just put the ADC right after the antenna?**

RF Transceiver Layout



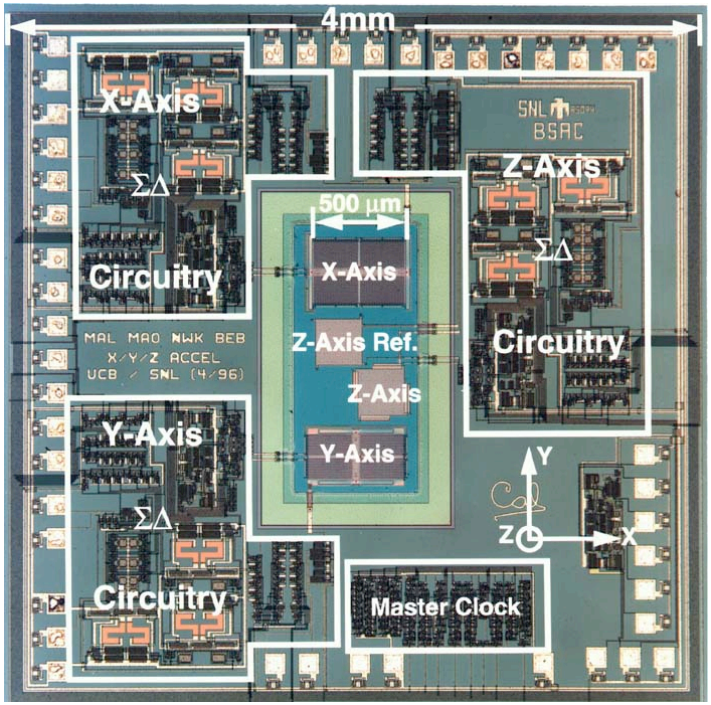




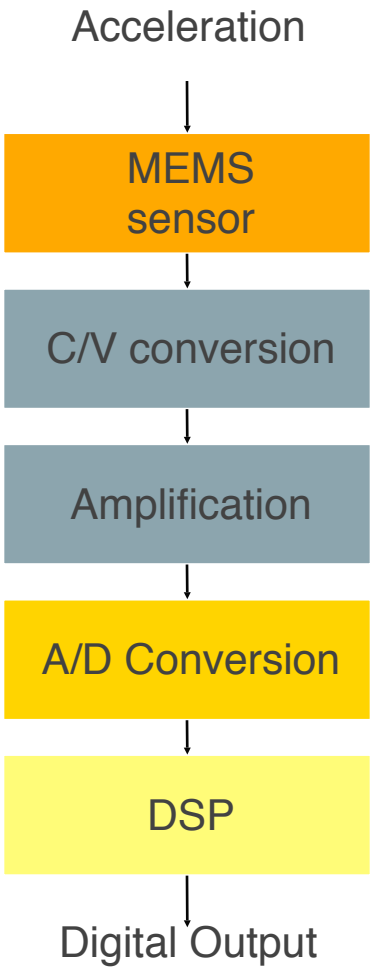
Source: Mehta et al, "An 802.11g WLAN SoC", JSSC Dec. 2005

- **Analog building blocks take up significant die area**
  - **Even in 0.18um…**

MEMS Accelerometer

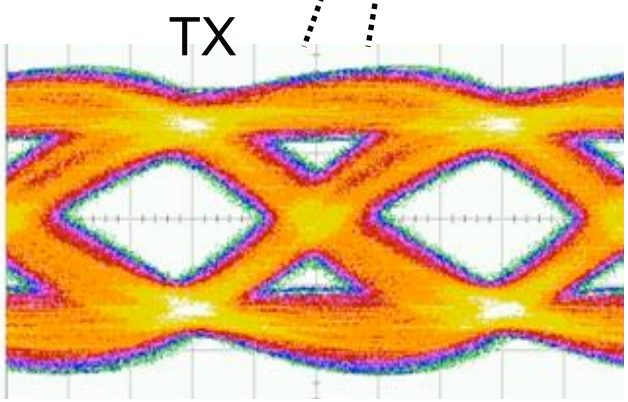


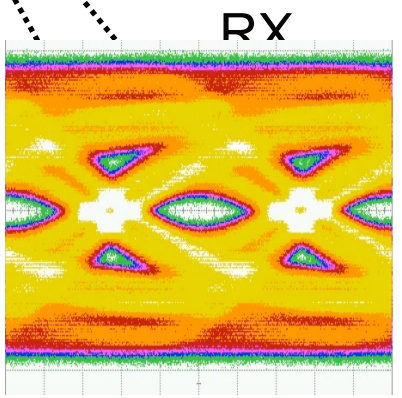
M. Lemkin and B. E. Boser, "A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics," IEEE J. Solid-State Circuits, vol. SC-34, pp. 456-468, April 1999



Another Example

- Look at interface between two digital chips
  - Is received bit a “1” or a “0”?
- Analog circuits critical for receiving bits correctly





Digital Versus Analog Design

- Abstraction in digital is Boolean logic (1's, 0's)
  - Works because of noise margins
- At a higher level, it's gates and registers (RTL)
- Digital layout is often automated

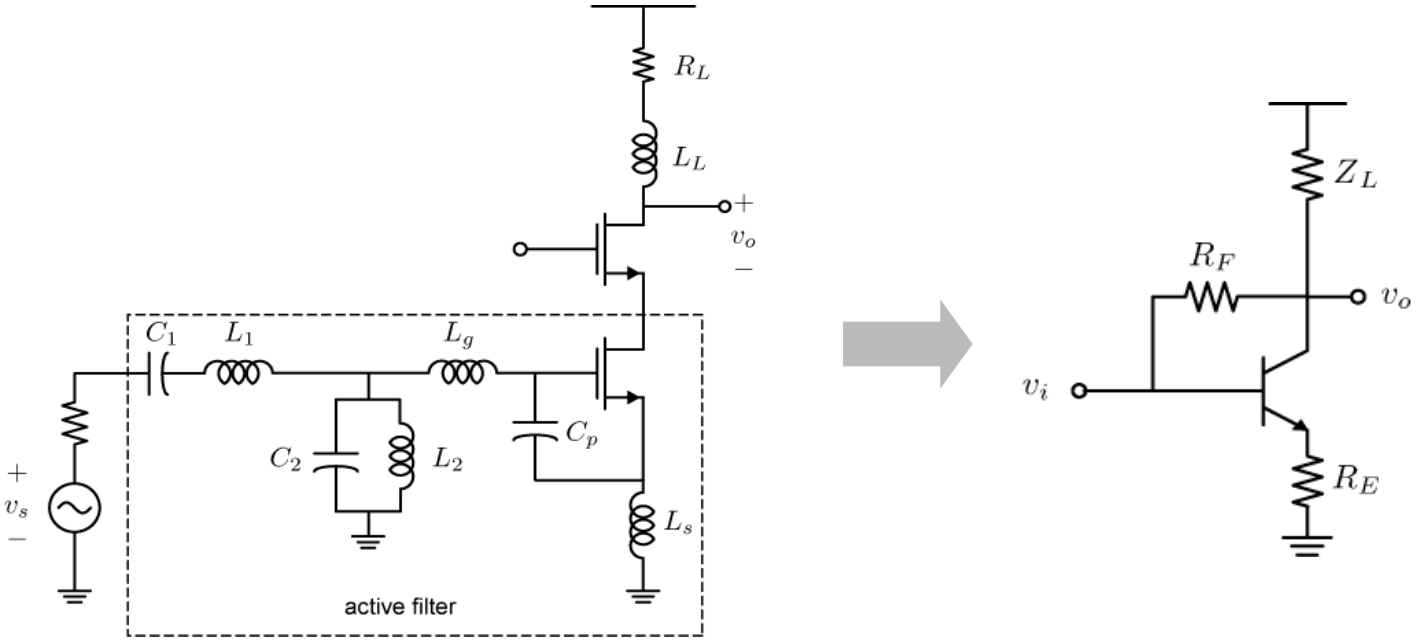
- Abstraction in analog is the device model
  - (BSIM is a few thousand lines long)
- At a higher level, it's the (opamps) (filters) (comparators)
  - Abstraction depends on the problem you're solving
- Analog layout is usually hand crafted

“Analog” versus “RF”

- RF = “Analog with inductors”
- RF signal is usually narrowband (i.e., sinusoidal)
  - Tuned circuit techniques used for signal processing.
- RF impedance levels are relatively low
  - Can’t make antenna impedance too high

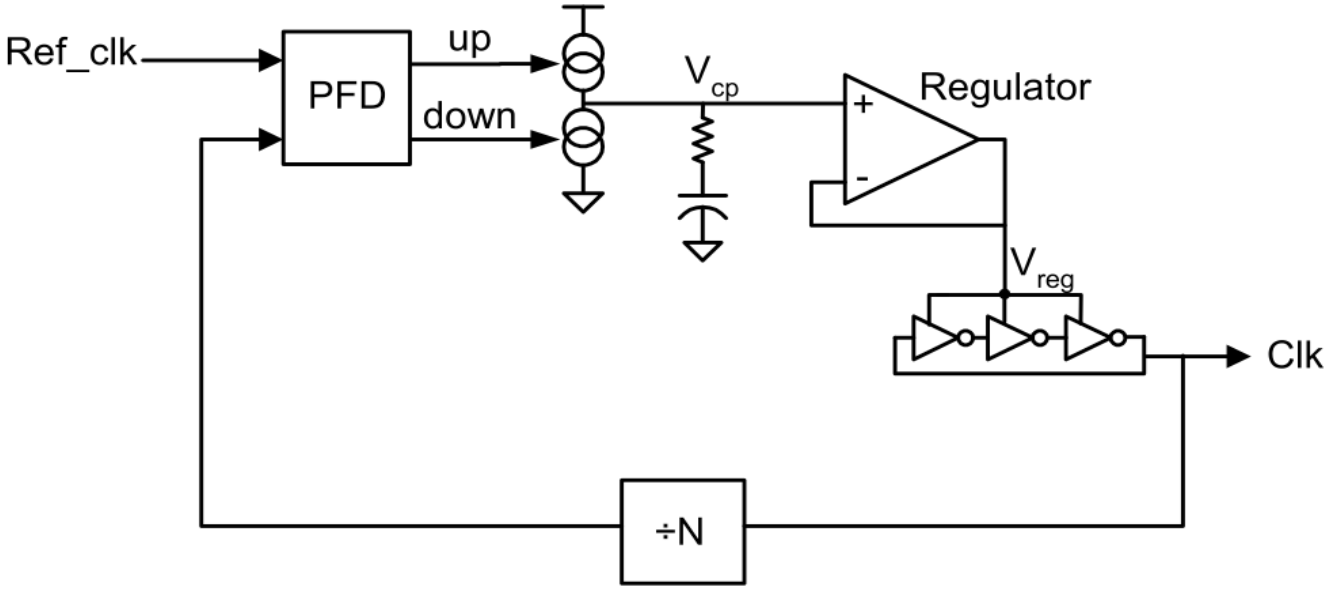
- Analog impedances are high (low) for voltage (current) gain.
  - Voltage/current gain versus power gain.
- “Mixed-signal” analog is often discrete time (sampled).

RF Shifting Toward Analog



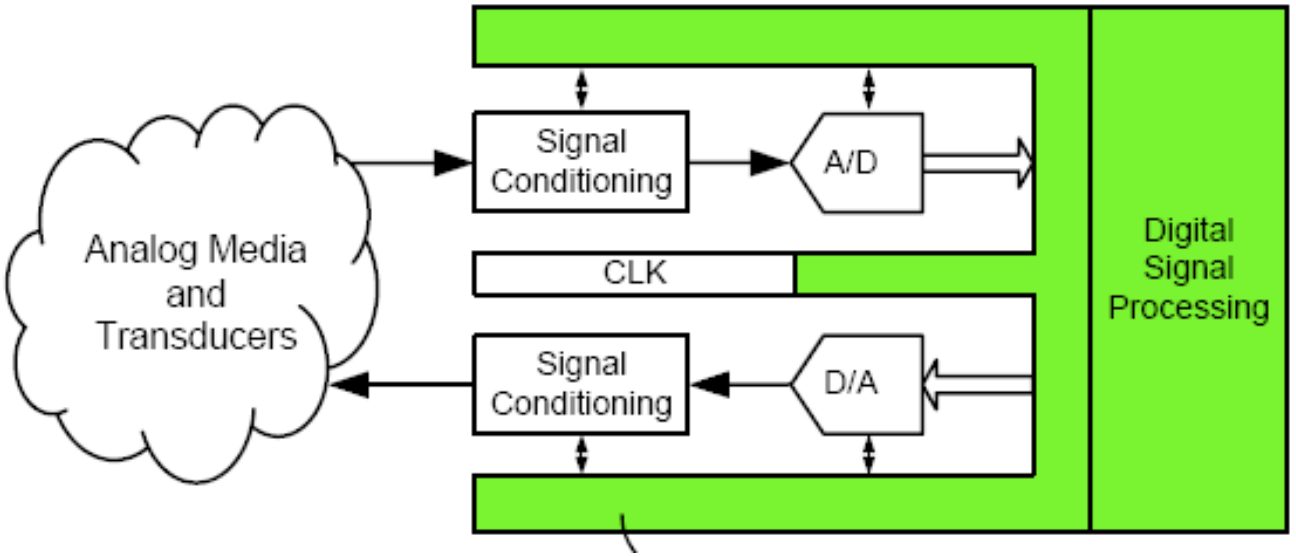
- **Classic RF uses inductors to tune the circuits**
  - **Inductors are big – would be nice to get rid of them**
- **With increasing f_T, moving towards wideband analog & feedback**
  - **What's the penalty?**

Mixed-Signal Design



- **Many building blocks involve analog and digital circuit co-design**
  - **PLLs, ADCs, etc.**
- **Sometimes hard to even distinguish between analog and digital**
  - **Is VCO analog, or digital?**

Digitally-Assisted Analog



Source: B. Murmann, "Digitally-Assisted Analog Circuits – A Motivational Overview," ISSCC 2007.

- **In 90nm, one RF inductor (200µ× 200µ) takes same area as a microprocessor!**
  - **Leverage digital processing to improve analog circuits**
- **Good analog design doesn't go away though**
  - **Need to find right partitioning to maximize the benefit**

Syllabus

- Devices (both passive and active):
  - Models, simulation, layout, and matching
- Electronic noise
- Basic support functions:
  - Current sources, references, biasing
- Basic analog “gate”: amplifier
  - Opamps, OTAs, feedback, settling time, common-mode feedback
- Application driver: A/D converters
  - Motivates additional building blocks
    - As well as why you care about certain specs
  - Data converters, comparators, offset cancellation, filters, sample & hold

EECS 240 versus 247

- EECS 240
  - Transistor level building blocks
  - Device and circuit fundamentals
  - A lot of the class at a low level of abstraction
    - SPICE/SPECTRE
- EECS 247
  - Macro-models, behavioral simulation, large systems
  - Signal processing fundamentals
  - High level of abstraction
  - Matlab

240 versus 242/142

- 142/242 mostly concerned with narrowband circuits operating at a “high” carrier frequency
  - Signals mostly look like sinusoids
  - Inductors ubiquitous
  - Use of feedback is rare

- 240 focuses on more “wideband”, general-purpose analog and mixed-signal
  - Signals are “arbitrary”
  - Spend a lot of time worrying about capacitance
  - Feedback common

240 versus 231

- 231 concentrates on device physics

- 240: device physics abstracted to the extent possible
  - Device models from a "circuit designer's perspective"
  - Treat transistor as black box described by complex equations
  - Equations relevant for biasing, nonlinear effects (output swing), and some charge storage effects
  - Mostly outside design loop
  - → "small signal analysis"